options to view or change settings, view trip history or activate utility features are not available with *flashSAFE* active. The user may deactivate *flashSAFE* by pressing the *EXIT* key. If *flashSAFE* has been activated through the optional switchbox or MODBUS communications, it must be deactivated through these means.

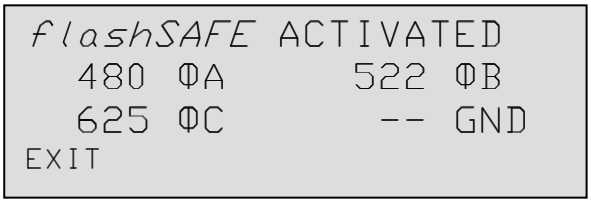

Figure 40, View of Display with *flashSAFE* Activated

2.6.2. Virtual Shunt Trip

If the *SHUNT TRIP FROM FRONT PANEL* option has been selected from the *OPTIONS* menu, the screen shown in figure 41 appears.

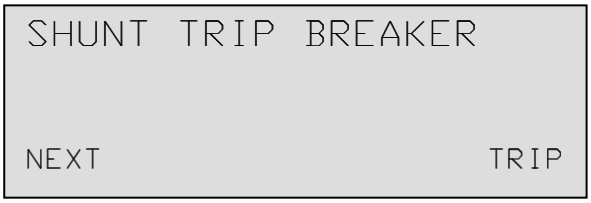

Figure 41, Virtual Shunt Trip Screen

Pressing the *TRIP* button causes the breaker to trip. Note that this function is not available if the breaker is equipped with an optional hardware interlock or if AC current is not high enough to exceed the threshold for self-power.

2.6.3. Test Mode

Test mode is entered through the *Utilities* menu from the screen shown in figure 42.

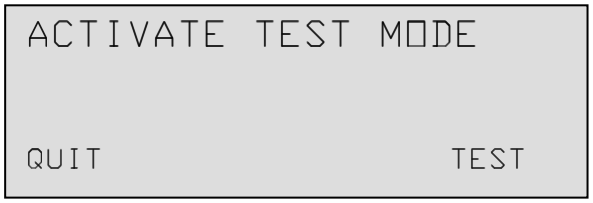

Figure 42, Test Mode Activation Screen

Test mode is intended as an aid to field technicians performing primary or secondary injection tests. It is recommended that all such testing be performed while in this mode. When test mode is activated, the screen shown in figure 43 is displayed and the following occurs:

- Logging of trips into trip log and count memory is suspended.
- The display timeout is increased to approximately 15 minutes.
- Thermal memory is disabled.
- Soft keys that allow the toggling of Short-Time, Instantaneous, Ground Fault and Phase Imbalance functions become available.
- "As found" settings are logged into permanent memory. These settings will be restored when test mode is exited.

IMPORTANT

When the *etc-12* is configured in *test* mode, it is vital to clear a trip using the softkey shown on the screen depicted in figure 44. The unit will not trip a second time until either the first trip is cleared or test mode is exited.

Note that this action is only necessary when in test mode. The breaker will function properly even if it is inadvertently placed in service without clearing a prior trip.

The *SETUP* and *UTILITIES* are also available from test mode. This allows for changing of settings and activation of *flashSAFE* or other features.

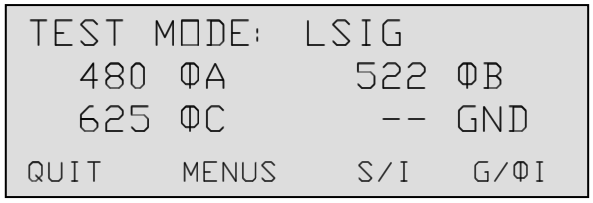

Figure 43, Test Mode Metering Screen

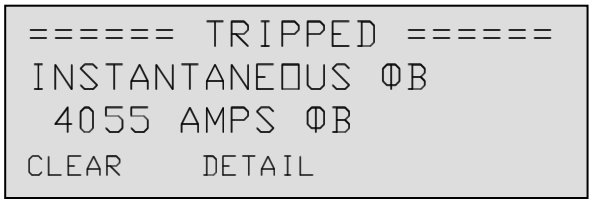

Figure 43, Test Mode Tripped Screen

Test mode can be exited through any the following methods:

1) Disconnecting the *ETD* display from the *etc-12.*
2) Allowing the timeout to occur by not pressing any buttons for 15 minutes.
3) Pressing the *QUIT* key.
4) Applying more than one phase of current to the *etc-12.*

After test mode is exited, “As found” settings are automatically restored and normal trip logging is resumed.

Refer to section 2.4 for further information regarding clearing the trip log and counter. Breaker information can be cleared as detailed in section 2.5. Recommended test procedures are described in the following section.

3.0 Testing

The *etc-12* programmers is designed to be field tested using either a primary injection test set or the Satin secondary injection test (*PTS*) coupled with the *etc-12 adapter*. It is not possible to perform secondary injection testing using the *PTS* without this adapter.

The very low output voltage and impedance of typical primary injection test sets can cause the test set to act erratically when testing an *etc-12* that is interfaced with low ratio current sensors (below 70:0.2A 400:1A). If primary injection is to be performed for these applications, the *etc-12* must be either receive supplemental power or be tested using a test set with a load bank and a minimum output voltage of 60 VAC. Contact factory for more details.

WARNING!!

To prevent electrical shock or injury, disconnect the breaker from all primary and secondary power sources and be sure that the breaker is open and charging springs are discharged before performing tests or troubleshooting.

It is strongly recommended that all breakers be fully performance tested before being placed into service. Prior to testing, breakers should be lubricated and adjusted per the original manufacturer's maintenance instructions. The following procedures are intended to serve as guidelines to allow individuals with breaker maintenance and testing experiences to evaluate retrofitted circuit breakers.

WARNING!!

Never energize a breaker with the wire harness disconnected from the *etc-12* programmer or from the current sensors. Also, do not disconnect the harness while the breaker is in service or being tested. Doing either will open-circuit the current sensors and allow dangerous and damaging voltage to develop.

Before applying current, always verify that there is a proper electrical connection between the current sensors and the wiring harness and between the wiring harness and the etc-12 programmer.

NOTE

It is recommended that all testing be performed while in test mode. Refer to section 2.6.3 for further information.

3.1. No Pickup Test

This test verifies that the *etc-12* will not improperly enter pickup or have the propensity to nuisance trip when monitored current is just slightly less than the set pickup value.

Procedure:

a) While in *TEST MODE,* disable ground fault and phase imbalance, as applicable.
b) Apply a current that has a magnitude of 90% of the long-time pickup value.
c) Allow the current to dwell for the period listed in table 4 while observing that the *etc-12* does not enter pickup or trip.
d) Repeat test for all three phases.
e) The unit passes if it does not enter pickup or trip at any time during this test.

TABLE 4, *No Trip Test* Durations	
LTD setting	**Test time in seconds**
MIN or custom from 1-9 sec	300
INT or custom from 10-20 sec	725
MAX or custom above 27 sec	1650

3.2. Long-Time Pickup Test

This test verifies that the *etc-12* programmer begins to count down for a long-time trip at the proper current value. This test requires checking the delay at three points.

Procedure:

a) While in *TEST MODE,* disable ground fault and phase imbalance, as applicable.
b) Slowly increase current from zero until the red pickup LED illuminates.
c) Verify that the LED turns on when current is between 90 and 113% of the long-time pickup value.
d) Repeat test for all three phases.

3.3. Long-Time Delay Test

This test verifies that the long-time delay characteristics meet the upper and lower limits. Delays are checked at three points along the delay band.

Procedure:

a) While in *TEST MODE,* disable ground fault, phase imbalance, short-time and instantaneous, as applicable.
b) Preset one of the test currents listed in table 5.
c) Apply test current and allow the programmer to count down and trip.
d) Verify that trip time conforms to the tolerances listed in table 5.
e) Repeat the test at each current level for all three phases.

TABLE 5, *Long Time Delay Test* Tolerances						
	I = 2X LTP		**I = 4X LTP**		**I = 6X LTP**	
LTD (sec @ 6x)	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**
1.0	7.64	10.52	1.91	2.63	0.85	1.17
1.5	11.45	15.78	2.86	3.95	1.27	1.75
2.0	15.27	21.04	3.82	5.26	1.70	2.34
2.5	19.09	26.30	4.77	6.58	2.12	2.92
3.0	22.91	31.57	5.73	7.89	2.55	3.51
3.5	26.72	36.83	6.68	9.21	2.97	4.09
4.0	30.54	42.09	7.64	10.52	3.39	4.68
4.5	34.36	47.35	8.59	11.84	3.82	5.26
5.0 (MIN)	38.18	52.61	9.54	13.15	4.24	5.85
6.0	45.81	63.13	11.45	15.78	5.09	7.01
7.0	53.45	73.65	13.36	18.41	5.94	8.18
8.0	61.08	84.17	15.27	21.04	6.79	9.35
9.0	68.72	94.70	17.18	23.67	7.64	10.52
10.0	76.35	105.22	19.09	26.30	8.48	11.69
11.0	83.99	115.74	21.00	28.94	9.33	12.86
12.0	91.62	126.26	22.91	31.57	10.18	14.03
13.0 (INT)	99.26	136.78	24.81	34.20	11.03	15.20
14.0	106.89	147.31	26.72	36.83	11.88	16.37
15.0	114.53	157.83	28.63	39.46	12.73	17.54
16.0	122.16	168.35	30.54	42.09	13.57	18.71
17.0	129.80	178.87	32.45	44.72	14.42	19.87
18.0	137.43	189.39	34.36	47.35	15.27	21.04
20.0	152.70	210.44	38.18	52.61	16.97	23.38
21.0	160.34	220.96	40.08	55.24	17.82	24.55
22.0	167.97	231.48	41.99	57.87	18.66	25.72
23.0	175.61	242.00	43.90	60.50	19.51	26.89
24.0	183.24	252.52	45.81	63.13	20.36	28.06
25.0	190.88	263.05	47.72	65.76	21.21	29.23
26.0	198.51	273.57	49.63	68.39	22.06	30.40
27.0 (MAX)	206.15	284.09	51.54	71.02	22.91	31.57
28.0	213.78	294.61	53.45	73.65	23.75	32.73
29.0	221.42	305.13	55.35	76.28	24.60	33.90
30.0	229.05	315.66	57.26	78.91	25.45	35.07

3.4. Instantaneous Pickup and Delay Test

This test verifies that instantaneous pickup and delay occur within tolerance. This requires measurement of the pickup point and the delay beyond the knee of the published curve.

Procedure:

a) While in *TEST MODE,* disable ground fault and phase imbalance, as applicable.
b) Refer to table 6 and preset the lower test current associated with the instantaneous pickup setting.
c) Apply short bursts of current and incrementally increase magnitude until an instantaneous trip occurs. This is the actual instantaneous pickup point and should fall between the upper and lower limits shown in table 6.
d) Preset a test current that is 150% of the value of the nominal instantaneous pickup setting.
e) Allow the *etc-12* to run at the test current. The programmer should trip within .050 seconds. Note that that the actual time to open the breaker is dependant upon the mechanical operation of the breaker. Additional adjustment and lubrication may be necessary if performance requirements are not met.
f) Repeat this test for each phase.

TABLE 6, *Instantaneous and Short Time* Pickup Tolerances

NOMINAL PICKUP	LOWER TOLERANCE LIMIT	UPPER TOLERANCE LIMIT
1.5L	1.35L	1.65L
2.0L	1.80L	2.20L
2.5L	2.25L	2.75L
3.0L	2.70L	3.30L
3.5L	3.15L	3.85L
4.0L	3.60L	4.40L
4.5L	4.05L	4.95L
5.0L	4.50L	5.50L
6.0L	5.40L	6.60L
7.0L	6.30L	7.70L
8.0L	7.20L	8.80L
9.0L	8.10L	9.90L
10.0L	9.00L	11.00L
11.0L	9.90L	12.10L
12.0L	10.80L	13.20L

3.5. Short Time Pickup Test

This test verifies that short-time pickup occurs within tolerance limits.

Procedure:

a) While in *TEST MODE,* disable ground fault and phase imbalance, as applicable.
b) Refer to table 6 and preset the lower test current associated with the short-time pickup setting.
c) Apply short bursts of current and incrementally increase magnitude until a short time trip occurs. This is the actual short-time pickup point and should fall between the upper and lower limits shown in table 6.
d) Repeat this test for each phase.

3.6. Short-Time Delay Test (I^2t off)

This test verifies that the constant mode short-time delay is within tolerance. The measurement is made 50% above the pickup setting. It is only necessary to verify one point on the curve when I^2t is set to off.

Procedure:

a) While in *TEST MODE,* disable ground fault and phase imbalance, and instantaneous as applicable.
b) Preset a test current that is 150% of the nominal short-time pickup setting.
c) Allow the *etc-12* to run at this test current.
d) Verify that the programmer trips within the tolerance limits described in table 7.
e) Repeat this test for each phase.

TABLE 7, *Short Time Delay* Tolerances with I^2t Off		
NOMINAL DELAY (s)	**LOWER TOLERANCE (s)**	**UPPER TOLERANCE (s)**
.070	.055	.125
.100	.068	.142
.150	.120	.192
.200	.170	.240
.300	.255	.345
.400	.340	.470
.500	.425	.585
.600	.510	.700
.700	.595	.905

3.7. Short-Time Delay Test (I^2t on)

This test verifies that the short-time I^2t delay is within tolerance. The delay trimming is verified at a current level that is between 125 and 150% of the pickup value. It is only necessary to check one point to verify this function.

Procedure:

a) While in *TEST MODE,* disable ground fault and phase imbalance, and instantaneous as applicable.
b) Preset a test current that is between 125 and 150% of the short time pickup value.
c) Allow the *etc-12* to run at this test current.
d) Verify that the programmer trips within the tolerance limits described in table 8.
e) Repeat test for each phase.

TABLE 8, Tolerances for *Short-time delay with I^2t ON*														
	I = 3L		**I = 4L**		**I = 5L**		**I = 6L**		**I = 7L**		**I = 8L**		**I = 9L**	
ST DELAY	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**
.070s	0.611	1.389	0.344	0.781	0.220	0.500	0.153	0.347	0.112	0.255	0.086	0.195	0.068	0.154
.100s	0.756	1.578	0.425	0.888	0.272	0.568	0.189	0.394	0.139	0.290	0.106	0.222	0.084	0.175
.150s	1.333	2.133	0.750	1.200	0.480	0.768	0.333	0.533	0.245	0.392	0.188	0.300	0.148	0.237
.200s	1.889	2.667	1.063	1.500	0.680	0.960	0.472	0.677	0.347	0.490	0.266	0.375	0.210	0.296
.300s	2.833	3.833	1.594	2.156	1.020	1.380	0.708	0.958	0.520	0.704	0.398	0.539	0.315	0.426
.400s	3.778	5.222	2.125	2.938	1.360	1.880	0.944	1.306	0.694	0.959	0.531	0.734	0.420	0.580
.500s	4.722	6.500	2.656	3.656	1.700	2.340	1.181	1.625	0.867	1.194	0.644	0.914	0.525	0.722
.600s	5.667	7.778	3.188	4.375	2.040	2.800	1.417	1.944	1.041	1.429	0.797	1.094	0.630	0.864
.700s	6.611	10.056	3.719	5.656	2.380	3.620	1.653	2.514	1.214	1.847	0.930	1.414	0.735	1.117
	TIME TO TRIP (SECONDS)													

3.8. Ground-Fault Pickup

This test verifies that ground-fault pickup occurs within tolerance limits.

Procedure:

e) While in *TEST MODE,* disable phase imbalance, if applicable.
f) Refer to table 9 and preset the lower test current associated with the ground-fault pickup setting.
g) Apply short bursts of current and incrementally increase magnitude until a ground fault trip occurs. This is the actual ground-fault pickup point and should fall between the upper and lower limits shown in table 9.
h) Repeat this test for each phase.

TABLE 9, *Ground-Fault* Pickup Tolerances

NOMINAL PICKUP	LOWER TOLERANCE LIMIT	UPPER TOLERANCE LIMIT
.10X	.07X	.14X
.15X	.11X	.20X
.20X	.17X	.23X
.25X	.22X	.28X
.30X	.26X	.34X
.35X	.30X	.40X
.40X	.35X	.45X
.45X	.39X	.51X
.50X	.44X	.57X
.55X	.48X	.62X
.60X	.52X	.68X
.65X	.57X	.73X
.70X	.61X	.79X
.75X	.65X	.85X
.80X	.70X	.90X
.85X	.74X	.96X
.90X	.78X	1.02X
.95X	.83X	1.07X
1.00X	.87X	1.13X
1.10X	.96X	1.24X
1.20X	1.04X	1.36X
1.30X	1.13X	1.47X
1.40X	1.22X	1.58X
1.50X	1.31X	1.70X
1.60X	1.39X	1.81X
1.70X	1.48X	1.92X
1.80X	1.57X	2.03X
1.90X	1.65X	2.15X
2.00X	1.74X	2.26X

3.9. Ground-Fault Delay (I^2t off)

This test verifies that the constant mode ground-fault delay is within tolerance. The measurement is made 100% above the pickup setting. It is only necessary to verify one point on the curve when I^2t is set to off.

Procedure:

a) While in *TEST MODE,* disable phase imbalance, if applicable.
b) Preset a test current that is 100% above the ground fault pickup.
c) Apply current and verify that the *etc-12* trips for ground fault within the tolerances described in table 10.
d) Repeat test for remaining phases.

TABLE 10, *Ground-Fault Delay* Tolerances with I^2t Off

NOMINAL DELAY (s)	LOWER TOLERANCE (s)	UPPER TOLERANCE (s)
.100	.068	.132
.150	.118	.182
.200	.168	.232
.300	.268	.332
.400	.350	.432
.500	.445	.532

3.10. Ground-Fault Delay (I^2t on)

This test verifies that the I^2t ground-fault delay is within tolerance. The measurement is made 150 to 200% above the pickup setting. It is only necessary to verify one point curve when I^2t is set to off.

Procedure:

a) While in *TEST MODE,* disable phase imbalance, if applicable.
b) Preset a test current that is between 150 and 200% of the short time pickup value.
c) Allow the *etc-12* to run at this test current.